CLAIMS

1. A method for fabricating variable quality substrate materials, the method comprising:

selecting a first mask having a first mask pattern;

projecting a laser beam through the first mask to anneal a first area of semiconductor substrate;

creating a first condition in the first area of the semiconductor film;

selecting a second mask having a second mask pattern;

projecting the laser beam through the second mask to anneal a second area of the semiconductor film; and,

creating a second condition in the second area of the semiconductor film, different than the first condition.

2. The method of claim 1 wherein creating a first condition in the first area of the semiconductor film includes creating crystalline material with a first lattice mismatch between adjacent crystal domains; and,

wherein creating a second condition in the second area of the semiconductor film includes creating crystalline material with a second lattice mismatch between adjacent crystal domains, less than the first lattice mismatch.

3. The method of claim 2 wherein creating crystalline material with a first lattice mismatch between adjacent crystal domains

includes forming a first number of high-angle grain boundaries per area; and,

wherein creating crystalline material with a second lattice mismatch between adjacent crystal domains, less than the first lattice mismatch, includes forming a second number of high-angle grain boundaries per area, smaller than the first number per area.

4. The method of claim 3 wherein forming a first number of high-angle grain boundaries per area includes forming a first number of high-angle grain boundaries per area with a crystal lattice mismatch angle in the range between 15 and 90 degrees; and,

wherein forming a second number of high-angle grain boundaries per area includes forming a second number of high-angle grain boundaries per area with a crystal lattice mismatch angle in the range between 15 and 90 degrees, less than the first number per area.

5. The method of claim 3 wherein forming a first number of high-angle grain boundaries per area includes forming adjacent high-angle grain boundaries separated by a first distance; and,

wherein forming a second number of high-angle grain boundaries per area includes forming adjacent high-angle grain boundaries separated by a second distance, greater than the first distance.

6. The method of claim 5 further comprising:

forming at least one transistor including a channel region in the second area; and,

forming at least one transistor including a channel region in the first area.

7. The method of claim 6 wherein forming the transistor in the second area includes completely forming a transistor channel region, having a length less than, or equal to the second distance, between adjacent high-angle grain boundaries.

8. The method of claim 7 wherein forming the transistor in the first area includes forming a transistor channel region, having a length greater than the first distance, including at least one high-angle grain boundary.

9. The method of claim 1 further comprising:

selecting a plurality of masks;

projecting the laser beam through each mask to anneal a corresponding area of semiconductor substrate; and,

creating a particular condition in each area of the semiconductor film.

10. The method of claim 1 wherein projecting the laser beam through the first mask to anneal a first area of semiconductor substrate includes using the first mask to laser anneal a plurality of nonadjacent regions of semiconductor film; and,

wherein projecting the laser beam through the second mask to anneal a second area of semiconductor substrate includes using the

second mask to laser anneal a plurality of nonadjacent regions of semiconductor film.

11. The method of claim 10 wherein using the first mask to laser anneal a plurality of nonadjacent regions of semiconductor film includes:

sequentially exposing each first area region to the projected laser beam;

sequentially annealing each of the nonadjacent regions of the first area.

12. The method of claim 10 further comprising:

establishing an order of adjacent regions across the semiconductor film;

aligning the laser beam with the semiconductor film in the established order;

wherein using the first mask to laser anneal a plurality of nonadjacent regions of semiconductor film includes projecting the laser beam through the first mask when the laser beam is aligned with a first area region; and,

wherein using the second mask to laser anneal a plurality of nonadjacent regions of semiconductor film includes projecting the laser beam through the second mask when the laser beam is aligned with a second area region.

13. A variable quality semiconductor film substrate comprising:

a first area with semiconductor film including crystalline material having a first lattice mismatch between adjacent crystal domains; and,

a second area with semiconductor film including crystalline material having a second lattice mismatch between adjacent crystal domains, less than the first lattice mismatch.

14. The substrate of claim 13 further comprising:

a plurality of areas with semiconductor film including crystalline material, each area having a particular degree of lattice mismatch between adjacent crystal domains.

15. The substrate of claim 13 wherein the first area includes a first number of high-angle grain boundaries per area; and,

wherein the second area includes a second number of high-angle grain boundaries per area, smaller than the first number per area.

16. The substrate of claim 15 wherein the first area includes a first number of high-angle grain boundaries per areas with a crystal lattice mismatch angle in the range between 15 and 90 degrees; and,

wherein the second area includes a second number of high-angle grain boundaries per areas with a crystal lattice mismatch angle in the range between 15 and 90 degrees, less than the first number per area.

17. The substrate of claim 15 wherein the first area includes adjacent high-angle grain boundaries separated by a first distance; and,

wherein the second area includes adjacent high-angle grain boundaries separated by second distance, greater than the first distance.

18. The substrate of claim 17 further comprising:

at least one transistor including a channel region formed in the second area; and,

at least one transistor including a channel region formed in the first area.

19. The substrate of claim 18 wherein the second area transistor channel region has a length less than, or equal to the second distance, completely formed between adjacent high-angle grain boundaries.

20. The substrate of claim 19 wherein the first area transistor channel region has a length greater than the first distance, including at least one high-angle grain boundary.

21. The substrate of claim 13 wherein the semiconductor film is silicon.

22. A polycrystalline silicon substrate including variable quality transistors, the substrate comprising:

a first area with at least one transistor having a channel region with a length greater than the distance between high-angle grain boundaries, including at least one high-angle grain boundary; and,

a second area with at least one transistor having a channel region with a length less than, or equal to the distance between high-angle grain boundaries, completely formed between adjacent high-angle grain boundaries.

23. A liquid crystal display (LCD) panel fabricated with a variable quality semiconductor film substrate, the panel comprising:

a first area including crystalline material having a first lattice mismatch between adjacent crystal domains; and,

a second area including crystalline material having a second lattice mismatch between adjacent crystal domains, less than the first lattice mismatch.

24. A liquid crystal display (LCD) panel fabricated with a variable quality semiconductor film substrate, the panel comprising:

a pixel array substrate area including crystalline material having a first lattice mismatch between adjacent crystal domains;

a column drivers substrate area including crystalline material having a second lattice mismatch between adjacent crystal domains, less than the first lattice mismatch;

a row drivers substrate area including crystalline material having the third lattice mismatch between adjacent crystal domains, less than the first lattice mismatch; and,

an on-board memory substrate area including crystalline material having a fourth lattice mismatch between adjacent crystal domains, less than the second and third lattice mismatches.